

*C3  
W*  
*cont.*  
*B1*  
*P,8  
Fig. 9B*

a source region having the first conductive type and provided on the channel region, the source region is located substantially at a center of the channel region, and wherein the source region is isolated from the insulation film, wherein:

an impurity concentration of the channel region is equal to or less than an impurity concentration in the drift region, and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region.

#### REMARKS

Claims 1-4 and 12 are pending. By this Amendment, claims 5-10 and 14-19 are canceled, and claim 12 is amended. Reconsideration and allowance are respectfully requested in view of the above amendments and the following remarks.

The attached Appendix includes a marked-up copy of the amended claim (37 C.F.R. 1.121(c)(ii)).

#### Allowable Subject Matter

Applicant gratefully acknowledges that the Office Action indicates that claims 1-4 are allowed. However, for the reasons stated below, Applicant respectfully submits that claim 12 is also allowable.

#### Rejection Under 35 U.S.C. § 112, First Paragraph

The Office Action rejects claims 5-10, 12, 14 and 15 under 35 U.S.C. § 112, first paragraph, with respect to the written description requirement. Applicant respectfully traverses this rejection with respect to claim 12.

The Office Action asserts that the specification "never discloses a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region and the source region is located substantially at a center of the channel region as claimed in claim 12". Applicant respectfully disagrees with this assertion.

Particularly, the specification at page 5, lines 16-29, describes that a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region. In addition, the specification at page 9, first paragraph, in referring to "the above-mentioned embodiment," describes that the source region 220 is located substantially at a center of the channel region 215. Thus, it is clear that the specification provides support for the recitation in claim 12 of "the source region is located substantially at a center of the channel region and "a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region."

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As stated at MPEP 2163.02, "[t]he test for sufficiency of support in a parent application is whether the disclosure of the application relied upon 'reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter.' " As stated at MPEP 2163.04, "[t]he examiner has the initial burden of presenting evidence or reasons why persons skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims." Applicant submits that the Examiner has not met this initial burden, in that no reasons have been presented as to why persons skilled in the art would not recognize in the present application a description of the invention defined by claim 12. Accordingly, this rejection should be withdrawn.

The Office Action also asserts that the specification "never discloses an impurity concentration in the channel region (second conductive type) is equal to or less than an impurity concentration in the cathode region (first conductive type) as claimed in claim 12".

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However, claim 12 does not recite such language.

Accordingly, the specification provides a sufficient written description of the subject matter of claim 12. Therefore, Applicant respectfully requests that the rejection under 35 U.S.C. § 112, first paragraph be withdrawn.

Rejection Under 35 U.S.C. § 112, Second Paragraph

The Office Action rejects claims 9, 10, 12, 14 and 15 under 35 U.S.C. § 112, second paragraph.

Claim 12 is amended to recite "a gate region provided so as to surround at least the channel region via an insulation film," to provide strict antecedent basis for "the insulation film." Accordingly, instant claim 12 meets the requirements of 35 U.S.C. § 112, second paragraph. Therefore, Applicant respectfully requests that this rejection be withdrawn.

Rejections Under 35 U.S.C. § 102

1. The Office Action rejects claim 14 under 35 U.S.C. § 102(e) over Williams et al. This rejection is moot.
2. The Office Action rejects claim 16 under 35 U.S.C. § 102(e) over Terasawa.

This rejection is moot.

Rejection Under 35 U.S.C. § 103

The Office Action rejects claims 17-19 under 35 U.S.C. § 103(a) over Terasawa. This rejection is moot.

For the foregoing reasons, Applicant respectfully requests reconsideration and withdrawal of the rejections and prompt allowance of the pending claims.

Should the Examiner believe that anything further is desirable to place the application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned representative at the number listed below.

Respectfully submitted,



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Attachment:  
Appendix

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## APPENDIX

## Changes to Claims:

Claims 5-10 and 4-19 are canceled.

The following is a marked-up version of the amended claim:

12. (Twice Amended) A semiconductor device comprising:

a substrate having a first conductive type;

a drift region having the first conductive type and disposed on the substrate;

a channel region having a second conductive type different from the first conductive type and provided on the drift region;

a gate region provided so as to surround at least the channel region via an insulation film; and

a source region having the first conductive type and provided on the channel region, the source region is located substantially at a center of the channel region, and wherein the source region is isolated from the insulation film, wherein:

an impurity concentration of the channel region is equal to or less than an impurity concentration in the drift region, and a depletion layer forms over the entire channel region sandwiched between the gate region when a zero bias is applied to the gate region.